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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing of one example of the gestalt of operation of the 1st of this invention, and (a) is a top view and (b) is a sectional view in alignment with AA.
[Drawing 2] (a) - (d) is a sectional view of the order of a process which manufactures the semiconductor device of this example.
[Drawing 3] (a) is a top view in the process of drawing 2 (c), and (b) is drawing having shown alternatively the 1st layer metal wiring 11, the 2nd layer metal wiring 14a and 14b, the contact hole 10, and the through hole 13 from the top view of drawing 1 (a).
[Drawing 4] (a) is the top view of the 2nd example and (b) is a sectional view in alignment with AA.
[Drawing 5] (a) - (c) is the sectional view of the order of a production process of the 2nd example.
[Drawing 6] (a) is drawing of the 3rd example and (b) is drawing of the 4th example.
[Drawing 7] (a) is the top view of the 5th example and (b) is a sectional view in alignment with AA.
[Drawing 8] It is the sectional view of the 5th example.
[Drawing 9] (a) is a top view at the completion time of metal silicide formation of one example of the gestalt of operation of the 2nd of this invention, and (b) is a sectional view in the phase which the formation to the 2nd layer metal wiring containing an inductor completed.
[Drawing 10] (a) is the top view of the conventional example and (b) is a sectional view along AA cross section.
[Drawing 11] It is a top view in the phase where the metal silicide 108a and 108b in the conventional example was formed.
[Description of Notations]
1,101 P-type silicon substrate
2,102 Isolation oxide film
3,103 p mold well
4 Gate Oxide
5a, 5b, 105a, 105b Polish recon
6,106 Sidewall
7,107 n mold source drain field
8a, 8b, 8c, 8d, 108a, 108b, 108c Metal silicide
9,109 The 1st interlayer insulation film
10, 10a, 110 Contact hole
11,111 The 1st layer metal wiring
12,112 The 2nd interlayer insulation film
13,113 Through hole
14a, 14b, 114a, 114b The 2nd layer metal wiring
15,115 Slitting
100,200 Semiconductor device

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MEANS

[Means for Solving the Problem] In the semiconductor device with which the circuit where the active element to which the semiconductor device of invention of the 1st of this invention contains an MOS transistor in a semi-conductor substrate, and an inductor are intermingled was incorporated Between said inductors and said semi-conductor substrate front faces directly under said inductor The 1st shielding pattern which consists of electric conduction film which is prepared, is insulated from said semi-conductor substrate front face by the 1st insulator layer, is insulated from said inductor by the 2nd insulator layer, and has two or more concave slitting toward the inside from a rim section side face, It has the 2nd shielding pattern which has the connection field which it is prepared in the convex type field in which it had consistency in said slitting, and was prepared in said semi-conductor substrate front face, and metal silicide was formed, and said semi-conductor substrate front face, and said metal silicide is formed, and connects said two or more convex type fields.
[0010] Moreover, the semiconductor device of the 2nd invention is set to the semiconductor device with which the circuit where the active element which contains an MOS transistor in a semi-conductor substrate, and an inductor are intermingled was incorporated. The 1st shielding pattern which consists of metal silicide which is prepared in said semi-conductor substrate front face directly under said inductor, and has two or more concave slitting toward the inside from a rim section side face, It is prepared between said inductor and said semi-conductor substrate front face, insulate from said semi-conductor substrate front face by the 1st insulator layer, insulate from said inductor by the 2nd insulator layer, and it has consistency in said slitting. It has the 2nd shielding pattern which has the connection field which consists of convex [which was prepared in said semi-conductor substrate front face] type the electric conduction film and said electric conduction film, and connects said two or more convex type electric conduction film.
[0011]
[Embodiment of the Invention] Next, this invention is explained to a detail. The semiconductor device of the gestalt of operation of the 1st of this invention The 1st shielding pattern which consists of electric conduction film which is insulated from a silicon substrate surface by the 1st insulator layer, is insulated from an inductor by the 2nd insulator layer, and has two or more concave slitting toward the inside between an inductor and the silicon substrate surface directly under an inductor, It has the 2nd shielding pattern which has the connection field which connects the convex type field in which it was prepared in the silicon substrate surface, had consistency in concave slitting, and metal silicide was formed, and two or more convex type fields. Drawing 1 is drawing of one example of the gestalt of operation of the 1st of this invention, (a) is a top view and (b) is a sectional view in alignment with AA.
[0012] In the semiconductor device 200, an inductor is formed by spiral 2nd layer metal wiring 14b, the 1st and 2nd interlayer insulation films 9 and 12 which are the 2nd insulator layer are inserted directly under the, and polish recon 5b by which metal silicide 8b of metals, such as titanium, cobalt, or nickel, was formed in the front face is prepared as electric conduction film. The slitting 15 used as a crevice is formed in polish recon 5b, and the 1st shielding pattern is constituted. Polish recon 5b is insulated with the p-type silicon substrate 1 with the isolation oxide film 2 which is the 1st insulator layer, it has

consistency on the thickness extent outside of a sidewall 6 mostly from polish recon 5b, and slitting of the isolation oxide film 2 is formed.
[0013] Metal silicide 8d containing connection field 8d-2 of the metal silicide which connects between metal silicide 8d-1 of a convex type configuration and two or more d-convex type configuration metal silicide 81 with slitting 15 in the adjusted configuration is prepared in the front face of the p-type silicon substrate 1, and the 2nd shielding pattern is constituted.
[0014] Each of 1st shielding pattern of metal silicide 8b and 2nd metal silicide 8d shielding pattern is connected to the earth terminal which is not illustrated. Since the 1st shielding pattern or the 2nd shielding pattern exists between 2nd layer metal wiring 14b of an inductor, and the p-type silicon substrate 1, in order to prevent the fall of the quality factor by the eddy current, when much slitting is prepared, generating of the substrate noise by coupling of 2nd layer metal wiring 14b of an inductor and the p-type silicon substrate 1 can be prevented nearly completely.
[0015] The end of an inductor is connected to polish recon 5a which constitutes the gate electrode of an N-channel metal oxide semiconductor transistor through a through hole 13, the 1st layer metal wiring 11, and a contact hole 10. The isolation oxide film with which two separate electrically n mold source drain field 7 of an n channel MOS transistor, and the source drain field of other MOS transistors which are not illustrated among drawing, The metal silicide by which 3 was formed in p mold well for the sidewall of an insulator layer and 8a, and 6 was formed in the front face of polish recon 5a of the gate electrode of an MOS transistor, the metal silicide by which 8c was formed in the source drain field front face, and 14a show the 2nd layer metal wiring.
[0016] Drawing 2 (a) - (d) is a sectional view of the order of a process which manufactures the semiconductor device of this example. First, the isolation oxide film 2 is formed in the front face of the p-type silicon substrate 1 alternatively in thickness of 200-500nm. The isolation oxide film 2 is not formed in slitting formation schedule field 15a of an inductor formation field at this time (drawing 2 (a)).
[0017] Next, after forming the p well 3, sequential growth of the polish recon of 4,100-400nm of 2-10nm gate oxide is carried out, and polish recon 5a of a gate electrode is formed using a resist mask. At this time, polish recon 5b which cut deeply on the substrate of an inductor wiring formation field, and prepared 15 in coincidence is formed in coincidence. The insulator layer 201 for after [pattern formation] sidewalls of polish recon is grown up (drawing 2 (b)).
[0018] next, the source drain field 7 (and source drain field of p mold of the P channel MOS transistor which is not illustrated) of n mold after carrying out etchback of the insulator layer 201 for sidewalls and forming a sidewall 6 -- ion-implantation -- forming -- RTA (rapid thermal annealing) -- by law, heat treatment for 10 - 60 seconds is added at 1000-1100 degrees C, and the impurity of the source drain field 7 is activated. Then, the silicon front face and polish recon front face of a metal silicide formation schedule field are exposed, for example, cobalt is put and heat-treated, and metal silicide 8a, 8c, 8b, and 8d is formed in polish recon 5b of polish recon 5a of the gate section of an MOS transistor, n mold source drain field 7, and an inductor wiring formation schedule field, and p-type silicon substrate 1 front face of the field of slitting 15, respectively (drawing 2 (c)).
[0019] Then, the 1st interlayer insulation film 9 is grown up into the thickness of 800-1200nm (drawing 2 (d)), and a contact hole 10 is formed in a need part using a resist mask. After embedding metal membranes, such as a tungsten, in a contact hole 10, metal membranes, such as aluminum, are grown up into the thickness of 400-800nm, and the 1st layer metal wiring 11 is formed using a resist mask. Furthermore, the 2nd interlayer insulation film 12 is grown up to be the thickness of 800-1200nm, and a through hole 13 is formed in a need part using a resist mask. After embedding metal membranes, such as a tungsten, in a through hole 13, metal membranes, such as aluminum, are grown up into the thickness of 400-800nm, inductor wiring 14b of the 2nd layer metal wiring and wiring 14a for connection of the 2nd layer metal wiring are formed using a resist mask, and Fig. 1 (b) is obtained.
[0020] Drawing 3 (a) is a top view in the phase of drawing 2 (c). In drawing 3 (a), metal silicide 8a on polish recon 5a of a gate electrode and metal silicide 8b which constitutes the 1st shielding pattern on polish recon 5b directly under an inductor pattern Since it is the metal silicide by which all were formed

on polish recon, the lower left attaches hatching of ** in common.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, in this conventional example, it could not prevent that the high frequency current flowed from this part to the p-type silicon substrate 101 since the field of the slitting 115 of polish recon 105b is not shielded, but shielding nature had the rebellion-trouble of falling conversely as much slitting 115 was formed, in order to make control of an eddy current perfect.
[0008] The purpose of this invention is compatible in control of an eddy current the shielding disposition top between an inductor and a substrate, and solves the above-mentioned rebellion-trouble, and generating of a substrate noise can reduce it more, and it is to offer the semiconductor device which can suppress smaller the fall of the quality factor Q of the inductor by the eddy current.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the semiconductor device which carried the MOS transistor and the inductor about a semiconductor device.
[0002]
[Description of the Prior Art] In the semiconductor device for RF circuits, it is one of the important elements to raise the noise property of the whole RF circuit by decreasing the noise which a substrate generates. Since especially an inductor occupies a big substrate area compared with other circuit elements, the high frequency current flows to a substrate by coupling of the wiring layer pattern and the substrate [directly under] of it which constitute an inductor, and by resisted part of a substrate, it generates a noise in a substrate and has a bad influence on the property of a RF circuit. In order to control noise generating by coupling, the approach of preparing the conductive layer which consists of a metal silicide layer between an inductor pattern and a silicon substrate, grounding through metal wiring, and shielding is used, but since an eddy current occurs in a metal silicide layer, the problem that the quality factor Q of an inductor falls arises.
[0003] The structure of the inductor which aims at reduction in an eddy current by preparing slitting in a metal silicide layer as a conventional example which solves this is indicated by "1997 Symposium on VLSI Circuits Digest of Technical Papers and pp.85-86." Drawing 10 (a) is the top view of this conventional example, and (b) is a sectional view along AA cross section. Hereafter, the conventional example is explained with reference to drawing 10 (a) and (b).
[0004] In the semiconductor device 100, an inductor is formed by 2nd layer metal wiring 114b of a spiral inductor pattern, the 1st interlayer insulation film 109 and the 2nd interlayer insulation film 112 are inserted directly under it, and polish recon 105b by which metal silicide 108b of metals, such as titanium, cobalt, or nickel, was formed in the front face is prepared in it. Moreover, the concave slitting 115 is formed in polish recon 105b toward the interior from the rim section side face. The end of an inductor is connected to polish recon 105a which constitutes the gate electrode of an N-channel metal oxide semiconductor transistor through a through hole 113, the 1st layer metal wiring 111, and a contact hole 110. the inside of drawing, and 101 -- a p-type silicon substrate and 102 -- in an isolation oxide film and 103, p mold well and 106 show the sidewall of an insulator layer, and, as for n mold source drain field and 108c, 107 shows the 2nd layer metal wiring, as for metal silicide and 114a.
[0005] In order to make the description of the structure of the conventional example clearer, the top view in the phase where metal silicide 108a, 108b, and 108c was formed in drawing 11 is shown. In drawing 11 , since each of metal silicide 108a on polish recon 105a of a gate electrode and metal silicide 108b on polish recon 105b directly under an inductor pattern is the metal silicide formed on polish recon, in common, the lower left attached hatching of **, and the lower right has attached and distinguished hatching of ** to metal silicide 108c formed in n mold source drain field 107 top of an n channel MOS transistor, i.e., the silicon front face of a substrate.
[0006] According to this structure, since metal silicide layer 108b on polish recon 105b directly under an

inductor pattern is grounded, the noise generated in the p-type silicon substrate 101 can be reduced in remarkable extent, it cuts deeply to coincidence at polish recon 105b directly under an inductor pattern, and metal silicide layer 108b and 115 is prepared, it is possible to also control generating of an eddy current in remarkable extent.

[0007]

[Problem(s) to be Solved by the Invention] However, in this conventional example, it could not prevent that the high frequency current flowed from this part to the p-type silicon substrate 101 since the field of the slitting 115 of polish recon 105b is not shielded, but shielding nature had the rebellion-trouble of falling conversely as much slitting 115 was formed, in order to make control of an eddy current perfect.

[0008] The purpose of this invention is compatible in control of an eddy current the shielding disposition top between an inductor and a substrate, and solves the above-mentioned rebellion-trouble, and generating of a substrate noise can reduce it more, and it is to offer the semiconductor device which can suppress smaller the fall of the quality factor Q of the inductor by the eddy current.

[0009]

[Means for Solving the Problem] In the semiconductor device with which the circuit where the active element to which the semiconductor device of invention of the 1st of this invention contains an MOS transistor in a semi-conductor substrate, and an inductor are intermingled was incorporated Between said inductors and said semi-conductor substrate front faces directly under said inductor The 1st shielding pattern which consists of electric conduction film which is prepared, is insulated from said semi-conductor substrate front face by the 1st insulator layer, is insulated from said inductor by the 2nd insulator layer, and has two or more concave slitting toward the inside from a rim section side face, It has the 2nd shielding pattern which has the connection field which it is prepared in the convex type field in which it had consistency in said slitting, and was prepared in said semi-conductor substrate front face, and metal silicide was formed, and said semi-conductor substrate front face, and said metal silicide is formed, and connects said two or more convex type fields.

[0010] Moreover, the semiconductor device of the 2nd invention is set to the semiconductor device with which the circuit where the active element which contains an MOS transistor in a semi-conductor substrate, and an inductor are intermingled was incorporated. The 1st shielding pattern which consists of metal silicide which is prepared in said semi-conductor substrate front face directly under said inductor, and has two or more concave slitting toward the inside from a rim section side face, It is prepared between said inductor and said semi-conductor substrate front face, insulate from said semi-conductor substrate front face by the 1st insulator layer, insulate from said inductor by the 2nd insulator layer, and it has consistency in said slitting. It has the 2nd shielding pattern which has the connection field which consists of convex [which was prepared in said semi-conductor substrate front face] type the electric conduction film and said electric conduction film, and connects said two or more convex type electric conduction film.

[0011]

[Embodiment of the Invention] Next, this invention is explained to a detail. The semiconductor device of the gestalt of operation of the 1st of this invention The 1st shielding pattern which consists of electric conduction film which is insulated from a silicon substrate surface by the 1st insulator layer, is insulated from an inductor by the 2nd insulator layer, and has two or more concave slitting toward the inside between an inductor and the silicon substrate surface directly under an inductor, It has the 2nd shielding pattern which has the connection field which connects the convex type field in which it was prepared in the silicon substrate surface, had consistency in concave slitting, and metal silicide was formed, and two or more convex type fields. Drawing 1 is drawing of one example of the gestalt of operation of the 1st of this invention, (a) is a top view and (b) is a sectional view in alignment with AA.

[0012] In the semiconductor device 200, an inductor is formed by spiral 2nd layer metal wiring 14b, the 1st and 2nd interlayer insulation films 9 and 12 which are the 2nd insulator layer are inserted directly under the, and polish recon 5b by which metal silicide 8b of metals, such as titanium, cobalt, or nickel, was formed in the front face is prepared as electric conduction film. The slitting 15 used as a crevice is formed in polish recon 5b, and the 1st shielding pattern is constituted. Polish recon 5b is insulated with

the p-type silicon substrate 1 with the isolation oxide film 2 which is the 1st insulator layer, it has consistency on the thickness extent outside of a sidewall 6 mostly from polish recon 5b, and slitting of the isolation oxide film 2 is formed.

[0013] Metal silicide 8d containing connection field 8d-2 of the metal silicide which connects between metal silicide 8d-1 of a convex type configuration and two or more d-convex type configuration metal silicide 81 with slitting 15 in the adjusted configuration is prepared in the front face of the p-type silicon substrate 1, and the 2nd shielding pattern is constituted.

[0014] Each of 1st shielding pattern of metal silicide 8b and 2nd metal silicide 8d shielding pattern is connected to the earth terminal which is not illustrated. Since the 1st shielding pattern or the 2nd shielding pattern exists between 2nd layer metal wiring 14b of an inductor, and the p-type silicon substrate 1, in order to prevent the fall of the quality factor by the eddy current, when much slitting is prepared, generating of the substrate noise by coupling of 2nd layer metal wiring 14b of an inductor and the p-type silicon substrate 1 can be prevented nearly completely.

[0015] The end of an inductor is connected to polish recon 5a which constitutes the gate electrode of an N-channel metal oxide semiconductor transistor through a through hole 13, the 1st layer metal wiring 11, and a contact hole 10. The isolation oxide film with which two separate electrically n mold source drain field 7 of an n channel MOS transistor, and the source drain field of other MOS transistors which are not illustrated among drawing, The metal silicide by which 3 was formed in p mold well for the sidewall of an insulator layer and 8a, and 6 was formed in the front face of polish recon 5a of the gate electrode of an MOS transistor, the metal silicide by which 8c was formed in the source drain field front face, and 14a show the 2nd layer metal wiring.

[0016] Drawing 2 (a) - (d) is a sectional view of the order of a process which manufactures the semiconductor device of this example. First, the isolation oxide film 2 is formed in the front face of the p-type silicon substrate 1 alternatively in thickness of 200-500nm. The isolation oxide film 2 is not formed in slitting formation schedule field 15a of an inductor formation field at this time (drawing 2 (a)).

[0017] Next, after forming the p well 3, sequential growth of the polish recon of 4,100-400nm of 2-10nm gate oxide is carried out, and polish recon 5a of a gate electrode is formed using a resist mask. At this time, polish recon 5b which cut deeply on the substrate of an inductor wiring formation field, and prepared 15 in coincidence is formed in coincidence. The insulator layer 201 for after [pattern formation] sidewalls of polish recon is grown up (drawing 2 (b)).

[0018] next, the source drain field 7 (and source drain field of p mold of the P channel MOS transistor which is not illustrated) of n mold after carrying out etchback of the insulator layer 201 for sidewalls and forming a sidewall 6 -- ion-implantation -- forming -- RTA (rapid thermal annealing) -- by law, heat treatment for 10 - 60 seconds is added at 1000-1100 degrees C, and the impurity of the source drain field 7 is activated. Then, the silicon front face and polish recon front face of a metal silicide formation schedule field are exposed, for example, cobalt is put and heat-treated, and metal silicide 8a, 8c, 8b, and 8d is formed in polish recon 5b of polish recon 5a of the gate section of an MOS transistor, n mold source drain field 7, and an inductor wiring formation schedule field, and p-type silicon substrate 1 front face of the field of slitting 15, respectively (drawing 2 (c)).

[0019] Then, the 1st interlayer insulation film 9 is grown up into the thickness of 800-1200nm (drawing 2 (d)), and a contact hole 10 is formed in a need part using a resist mask. After embedding metal membranes, such as a tungsten, in a contact hole 10, metal membranes, such as aluminum, are grown up into the thickness of 400-800nm, and the 1st layer metal wiring 11 is formed using a resist mask. Furthermore, the 2nd interlayer insulation film 12 is grown up to be the thickness of 800-1200nm, and a through hole 13 is formed in a need part using a resist mask. After embedding metal membranes, such as a tungsten, in a through hole 13, metal membranes, such as aluminum, are grown up into the thickness of 400-800nm, inductor wiring 14b of the 2nd layer metal wiring and wiring 14a for connection of the 2nd layer metal wiring are formed using a resist mask, and Fig. 1 (b) is obtained.

[0020] Drawing 3 (a) is a top view in the phase of drawing 2 (c). In drawing 3 (a), metal silicide 8a on polish recon 5a of a gate electrode and metal silicide 8b which constitutes the 1st shielding pattern on

polish recon 5b directly under an inductor pattern Since it is the metal silicide by which all were formed on polish recon, the lower left attaches hatching.of ** in common. Metal silicide 8d which is formed in a field including the p-type silicon substrate front face of the convex type field which cut deeply with metal silicide 8c formed on n mold source drain field 7 of an N-channel metal oxide semiconductor transistor, and was adjusted in 15, and constitutes the 2nd shielding pattern Since it is the metal silicide by which all were formed in the silicon front face of a substrate, the lower right has attached and distinguished hatching of ** in common. Metal silicide 8b and 8d is grounded through the earth terminal which is not illustrated.

[0021] Drawing 3 (b) is drawing having shown alternatively the 1st layer metal wiring 11, the 2nd layer metal wiring 14a and 14b, the contact hole 10, and the through hole 13 from the top view of drawing 1 (a). An inductor is formed in the shape of spiral shape, as 2nd layer metal wiring 14b shows.

[0022] Not only in the field covered by metal silicide layer 8b formed in the polish recon 5b front face which constitutes the 1st shielding pattern from a gestalt of this operation Since 8d of silicide layers which were prepared in the 1st shielding pattern and from which it cuts deeply and even the field of 15 constitutes the 2nd shielding pattern shields, Since coupling of an inductor and a silicon substrate is intercepted nearly completely Since 8d of metal silicide layers of the field of the slitting 15 which constitutes metal silicide layer 8b and the 2nd shielding pattern which constitute the 1st shielding pattern is separated by the sidewall 6 at least while being able to control noise generating with a substrate effectively Generating of an eddy current can be controlled and it can be compatible also in improvement in the quality factor Q of an inductor.

[0023] Drawing 4 (a) is the top view of the 2nd example, and (b) is a sectional view in alignment with AA. In this example, the point using the gate oxide 4 of an MOS transistor as the 1st insulator layer between polish recon 5b directly under an inductor and the p-type silicon substrate 1 differs from the 1st example of drawing 1 . Since the 1st shielding pattern or the 2nd shielding pattern exists like the 1st example also in this example between 2nd layer metal wiring 14b of an inductor, and the p-type silicon substrate 1, when much slitting is prepared for eddy current control, coupling of 2nd layer metal wiring 14b of an inductor and the p-type silicon substrate 1 can be prevented nearly completely. Moreover, since metal silicide 8b and metal silicide 8d can be formed in self align, consistency can be made to have with a sufficient precision with the structure of this example more easily than the 1st example.

[0024] Drawing 5 (a) - (c) is the sectional view of the order of a production process of the 2nd example. Drawing 2 (a) Although the structure of an inductor formation field differs from - (C), as a production process, it is the same.

[0025] Drawing 5 (a) is a sectional view after isolation oxide-film 2 formation as well as drawing 2 (a), and the point which does not form an isolation oxide film in an inductor formation field differs from drawing 2 (a).

[0026] Drawing 5 (b) is a sectional view after growing up the insulator layer 201 for sidewalls as well as drawing 2 (b), and it differs from drawing 2 (b) in that polish recon 5b of an inductor formation field is installed on gate oxide 4.

[0027] Drawing 5 (c) is a sectional view after metal silicide formation as well as drawing 2 (c). When the metal silicide 8a and 8c of the transistor section is formed in self align, similarly, metal silicide 8b formed on polish recon 5b also in an inductor formation field, and metal silicide 8d formed in the front face of the p-type silicon substrate 1, only spacing of a sidewall 6 is left and the point formed by having consistency in self align differs from drawing 2 (c).

[0028] Drawing 6 (a) and (b) are drawings of the 3rd and 4th example. Like drawing 6 (a), metal silicide 8d directly under an inductor may be formed in the front face of the same n mold field 7a as n mold source drain field 7 of an n channel MOS transistor, and p mold well 3a may be excluded. Moreover, you may form in the front face of the p mold field 202 same like drawing 6 (b) as p mold source drain of the p channel MOS transistor which is not illustrating metal silicide 8d.

[0029] Drawing 7 (a) is the top view of the 5th example, and (b) is a sectional view in alignment with AA. Moreover, drawing 8 is a sectional view in the phase which went to inductor formation. It straddled in 8d of metal silicide layers of p semi-conductor substrate 1 front face which constitutes metal silicide

layer 8b of a polish recon 5b front face and the 2nd shielding pattern which constitute the 1st shielding pattern from this example, and contact hole 10a is prepared. After forming the contact opening 204 like drawing 7 (b), when embedding metals, such as a tungsten, in the contact hole 10 of an MOS transistor, contact hole 10a is also embedded at coincidence, and the 1st shielding pattern and the 2nd shielding pattern are connected. Since what is necessary is just to connect either the 1st shielding pattern or the 2nd shielding pattern to an earth terminal in this example, wiring is reducible.

[0030] Next, the gestalt of operation of the 2nd of this invention is explained. The 1st shielding pattern which consists of metal silicide which the semiconductor device of the gestalt of this operation is formed in the silicon substrate surface directly under an inductor, and has two or more concave slitting toward the inside, It is prepared between an inductor and a silicon substrate surface, insulate from a silicon substrate surface by the 1st insulator layer, and it insulates from the inductor by the 2nd insulator layer. It has the 2nd shielding pattern which has the connection electric conduction film which connects the convex type electric conduction film prepared in concave slitting of the 1st shielding pattern by having consistency, and two or more convex type electric conduction film.

[0031] Drawing 9 (a) is the top view of the completion phase of metal silicide formation of one example of the gestalt of operation of the 2nd of this invention, and corresponds to drawing 3 in the gestalt of the 1st operation. Drawing 9 (b) is a sectional view in the time of formation to the 2nd layer metal wiring containing an inductor being completed, and corresponds to drawing 1 (b). In drawing 9 (a), the lower left gives the slash of ** to the metal silicide 8c and 8d which the lower right gave the slash of ** to the metal silicide 8a and 8b formed in the front face of polish recon like drawing 3 , and was formed on the surface of the silicon substrate at it.

[0032] In this example, it consists of metal silicide 8d by which the 1st shielding pattern which has the concave slitting 203 was formed in the front face of the p-type silicon substrate 1, and only the point which is metal silicide 8b by which the 2nd shielding pattern which has heights 8b-1 adjusted in concave slitting and connection field 8b-2 was formed in the polish recon 5b front face differs from the example of drawing 1 (b) and drawing 3 .

[0033] Since the 1st shielding pattern which has concave slitting occupies a usually bigger area than the 2nd shielding pattern which has a convex part, by forming the 1st shielding pattern of a large area in a silicon substrate surface like this example, it can reduce the total parasitic capacitance between the inductor, 1st, and 2nd shielding patterns, and is effective in the ability to enlarge resonance frequency of an inductor.

[0034] Also in the gestalt of this operation, like the gestalt of the 1st operation, it may change to the isolation oxide film 2 in drawing 9 (b) as the 1st insulator layer of the lower part of the polish recon film like drawing 4 , and gate oxide may be used. Moreover, it cannot be overemphasized that the silicon substrate surface in which lower of 1st shielding pattern, i.e., metal silicide, 8d is formed may be n mold like drawing 6 (a), or you may be p mold like drawing 6 (b). Moreover, the same is said of the wiring number to an earth terminal being reducible by forming the contact hole which straddles metal silicide 8d which constitutes the 1st shielding pattern like drawing 7 , and metal silicide layer 8b which constitutes the 2nd shielding pattern, embedding metal membranes, such as a tungsten, and connecting.

[0035]

[Effect of the Invention] As stated above, in invention of the 1st of this invention Since coupling of an inductor and a silicon substrate can intercept nearly completely with the 1st and 2nd shielding patterns While being able to control generating of the noise in a substrate effectively Since the metal silicide layer which constitutes the 1st shielding pattern, and the metal silicide layer of the field of slitting which constitutes the 2nd shielding pattern are separated by the sidewall of an insulator layer Generating of an eddy current can be controlled and it can be compatible also in improvement in the quality factor Q of an inductor.

[0036] Moreover, by applying invention of the 2nd of this invention, in addition to the above-mentioned effectiveness, the total parasitic capacitance between the inductor, 1st, and 2nd shielding patterns can be reduced, and the effectiveness that resonance frequency of an inductor can be enlarged arises.

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PRIOR ART

[Description of the Prior Art] In the semiconductor device for RF circuits, it is one of the important elements to raise the noise property of the whole RF circuit by decreasing the noise which a substrate generates. Since especially an inductor occupies a big substrate area compared with other circuit elements, the high frequency current flows to a substrate by coupling of the wiring layer pattern and the substrate [directly under] of it which constitute an inductor, and by resisted part of a substrate, it generates a noise in a substrate and has a bad influence on the property of a RF circuit. In order to control noise generating by coupling, the approach of preparing the conductive layer which consists of a metal silicide layer between an inductor pattern and a silicon substrate, grounding through metal wiring, and shielding is used, but since an eddy current occurs in a metal silicide layer, the problem that the quality factor Q of an inductor falls arises.
[0003] The structure of the inductor which aims at reduction in an eddy current by preparing slitting in a metal silicide layer as a conventional example which solves this is indicated by "1997 Symposium on VLSI Circuits Digest of Technical Papers and pp.85-86." Drawing 10 (a) is the top view of this conventional example, and (b) is a sectional view along AA cross section. Hereafter, the conventional example is explained with reference to drawing 10 (a) and (b).
[0004] In the semiconductor device 100, an inductor is formed by 2nd layer metal wiring 114b of a spiral inductor pattern, the 1st interlayer insulation film 109 and the 2nd interlayer insulation film 112 are inserted directly under it, and polish recon 105b by which metal silicide 108b of metals, such as titanium, cobalt, or nickel, was formed in the front face is prepared in it. Moreover, the concave slitting 115 is formed in polish recon 105b toward the interior from the rim section side face. The end of an inductor is connected to polish recon 105a which constitutes the gate electrode of an N-channel metal oxide semiconductor transistor through a through hole 113, the 1st layer metal wiring 111, and a contact hole 110. the inside of drawing, and 101 -- a p-type silicon substrate and 102 -- in an isolation oxide film and 103, p mold well and 106 show the sidewall of an insulator layer, and, as for n mold source drain field and 108c, 107 shows the 2nd layer metal wiring, as for metal silicide and 114a.
[0005] In order to make the description of the structure of the conventional example clearer, the top view in the phase where metal silicide 108a, 108b, and 108c was formed in drawing 11 is shown. In drawing 11 , since each of metal silicide 108a on polish recon 105a of a gate electrode and metal silicide 108b on polish recon 105b directly under an inductor pattern is the metal silicide formed on polish recon, in common, the lower left attached hatching of **, and the lower right has attached and distinguished hatching of ** to metal silicide 108c formed in n mold source drain field 107 top of an n channel MOS transistor, i.e., the silicon front face of a substrate.
[0006] According to this structure, since metal silicide layer 108b on polish recon 105b directly under an inductor pattern is grounded, the noise generated in the p-type silicon substrate 101 can be reduced in remarkable extent, it cuts deeply to coincidence at polish recon 105b directly under an inductor pattern, and metal silicide layer 108b and 115 is prepared, it is possible to also control generating of an eddy current in remarkable extent.

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EFFECT OF THE INVENTION

[Effect of the Invention] As stated above, in invention of the 1st of this invention Since coupling of an inductor and a silicon substrate can intercept nearly completely with the 1st and 2nd shielding patterns While being able to control generating of the noise in a substrate effectively Since the metal silicide layer which constitutes the 1st shielding pattern, and the metal silicide layer of the field of slitting which constitutes the 2nd shielding pattern are separated by the sidewall of an insulator layer Generating of an eddy current can be controlled and it can be compatible also in improvement in the quality factor Q of an inductor.
[0036] Moreover, by applying invention of the 2nd of this invention, in addition to the above-mentioned effectiveness, the total parasitic capacitance between the inductor, 1st, and 2nd shielding patterns can be reduced, and the effectiveness that resonance frequency of an inductor can be enlarged arises.

[Translation done.]